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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/065,365	10/09/2002	Robert W. Bassett	BUR920010209	7874

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EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 04/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/065,365	BASSETT ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 October 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-10 are presented for examination.

Claim Objections

The amendment received October 4, 2004 has overcome the previous Claim Objections, and those rejections are therefore withdrawn.

Claim Rejections - 35 USC § 112

The amendment received October 4, 2004 has overcome the previous 35 USC § 112 rejections and those rejections are therefore withdrawn.

Response to Arguments

Applicant's arguments filed October 4, 2004 have been fully considered but they are not persuasive.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "Applicants invention does not require the custom design of logic controls that are specific to each design" page 13 paragraph 3) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Applicants' arguments fail to comply with 37

CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "Applicants invention does not connect multiple pins of the device under test to a single tester channel. Applicants' invention does not Instead, Applicants' invention permits more than one stimulus per test pattern on the external I/O pins through repeated simulation. Any and all of the pins in the active bank can have stimuli applied by one of the re-simulated test patterns" page 13 paragraph 4) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Applicant's arguments do not comply with 37 CFR 1.111(c) because they do not clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. Further, they do not show how the amendments avoid such references or objections.

As such, the previous art rejection is maintained.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1 are rejected under 35 U.S.C. 103(a) as being obvious over Ellison et al. U.S. Patent No. 6,448,796 in view of Schnurmann U.S. Patten No. 5,348,759.

As per claims 1, and 2, Ellison et al. substantially teach the claimed method of parametric testing of high pin count circuits with low channel testers by the following; 1) identify all the types of common module drivers which can be grouped together at the tester interface board (TIB) or driver interface board (DIB). Grouping common drivers allows the parametric tests of the pins to use the same test criteria, and thus have a

consistent test for each of the shared pins at the connections. The test equipment can treat a shared pin as a consistent known entity and does not need to differentiate results based on patterns and type of driver. Typical designs tend to use common drivers across large busses and system interfaces, so this grouping is generally likely to be easily performed. 2) Insert logic driver controls in the design to allow only a single grouped driver of a grouping or bank to be active at any given test vector (column 3 line 50 through column 4 line 33, figure 3, claim 1). Not explicitly disclosed is applying test patterns from the tester.

However, in an analogous art, Schnurmann teaches a method for testing integrated circuits with less channels on the tester than pins on the integrated circuit and sending a test pattern through the pins. During operation, a plurality of terminal pins are connected to one channel. Each test pattern forces either a 0 or 1 to every input pin (column 8 lines 16-25, abstract, claims 1-5). Therefore, it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used the tester of Schnurmann with the method of Ellison et al. This would have been obvious as suggested by Ellison et al. (column 2 lines 7-15) in order to ensure high test coverage on high pin count products.

As per claim 3, Ellison et al. teach that grouping I/Os assists in being able to "fit " the device on a given test platform, but selective grouping, taking into account the physical I/O assignments and location, aids in minimizing test escapes to the field. Column 3 lines 5-13

As per claims 4-8, Ellison et al. teach Inserting driver logic controls is done at the chip design level, and requires I/O bank logic to uniquely control selected banks of I/O drivers. Taking the groups of common drivers into account, a suitable number of drivers are provided to facilitate an enable control function so as to allow specific control of any given driver bank. This design is then used to uniquely control the driver banks, when test vectors are created, by allowing selectively enabling drivers banks, and to control the number of I/Os which are switched for testing. (Column 3 line 66 through column 4 line 9, FIG. 3)

Claims 10 are rejected under 35 U.S.C. 103(a) as being obvious over Ellison et al. U.S. Patent No. 6,448,796 in view of Godiwala et al. U.S. Patent No. 5,712,858

As per claim 10, Ellison et al. substantially teach the claimed method of parametric testing of high pin count circuits with low channel testers by the following; 1) identify all the types of common module drivers which can be grouped together at the tester interface board (TIB) or driver interface board (DIB). Grouping common drivers allows the parametric tests of the pins to use the same test criteria, and thus have a consistent test for each of the shared pins at the connections. The test equipment can treat a shared pin as a consistent known entity and does not need to differentiate results based on patterns and type of driver. Typical designs tend to use common drivers across large busses and system interfaces, so this grouping is generally likely to be easily performed. 2) Insert logic driver controls in the design to allow only a single grouped driver of a grouping or bank to be active at any given test vector (column 3 line

50 through column 4 line 33, figure 3, claim 1). Not explicitly disclosed is applying test patterns to the ASIC from the tester.

However, in an analogous art, Godiwala et al. teach an electronic testing system for ASIC integrated circuits can test an electronic device which has more signal pins or pads (i.e., contacts) than the maximum number of tester probes. The testing system connects the contacts to the tester such that groups of contacts share individual tester signal lines. The testing system uses special selector logic on the device to be tested to determine which particular contacts of the groups are "currently output active", or capable of transmitting data. At each step in the testing procedure, the system can vary the sets of contacts which are chosen to be currently output active, thereby resulting in a high percentage of the possible states of the device being tested. The test system can apply precision voltage and current signals to the DUT contacts, and can measure precision voltage and current responses on those contacts to those applied signals. More specifically, the DUT is `exercised` by the test system by the application of a pattern of `ones` and `zeros`, or high and low voltages, known as a stimulus vector, on a selected set of the tester probes associated with that vector. Then the test system measures the DUTs output pattern of high and lows on a selected set of the DUT contacts associated with that vector, and compares this pattern to a predetermined, i.e. expected, pattern for that vector. (Column 4 lines 16-32, Abstract, claims 1-5,Figures 5,and 6) Therefore, it would have been obvious to a person having ordinary skill in the art to have used the method of Ellison et al. with the tester of Godiwala et al. This would

have been obvious as suggested by Ellison et al. (column 2 lines 7-15) in order to ensure high test coverage on high pin count products.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C Britt

Cynthia Britt
Examiner
Art Unit 2133

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